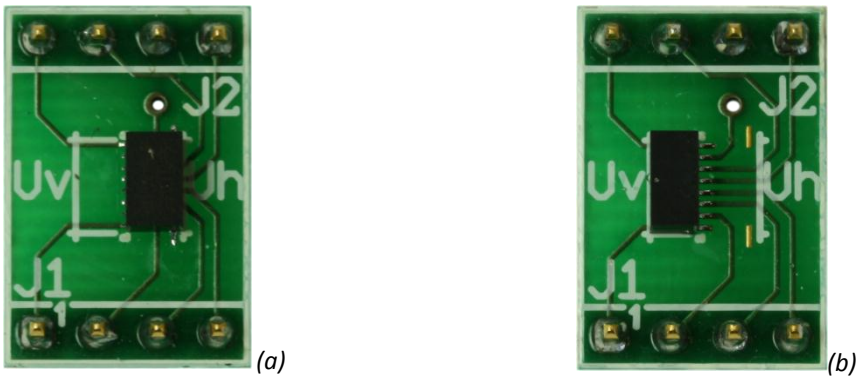
XEN1210 Experimentation boards

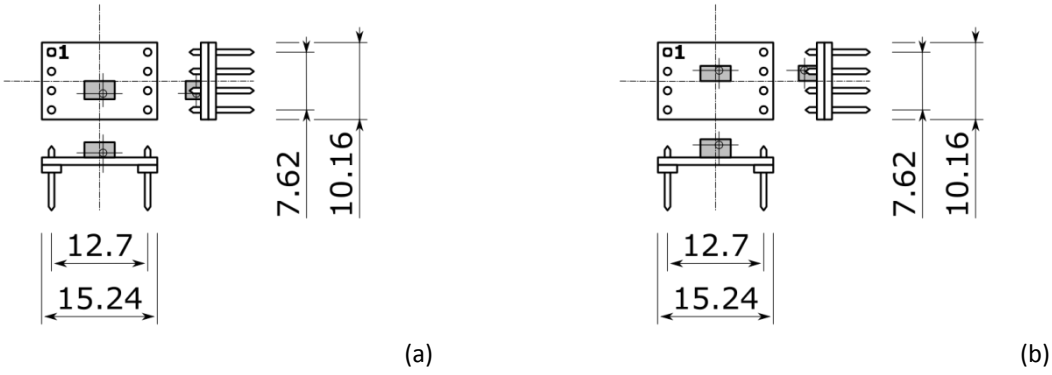


(a) (b)

Figure 1: An experimentation board is available for two magnetic directions, Z axis (a) and Y axis (b).

Table 1: XEN-1210-3D board pin definition.

Pin	Name	Type	Functionality
8	CLK	Dig. In	CLocK is the main clock and determines the speed of the module. Typical clock frequency is 1-5MHz.
6	SCK	Dig. In	Serial shift ClocK determines the speed of the SDI/SDO shift register.
7	CS	Dig. In	Chip Select selects the device when this input is low. A high level deselects the device and forces SDO into tri-state mode
5	SDI	Dig. In	Serial Data Input pin. Data shifted in is committed on the falling edge of SCK.
4	SDO	Tri-state Out	Serial Data Output pin. Data is shifted out on the positive edge of SCK.
3	DV	Dig. Out	The Data Valid pin is pulled down for one clock period when the internal shift register is refreshed with new data. It can be used as an interrupt signal for the host CPU. DV pins cannot be shared.
2	GND	Power	Analog and Digital Ground
1	VDD	Power	Analog and Digital Power Supply (2.5V - 3.3V)



(a) (b)

Figure 2: An experimentation board is available for two magnetic directions, Z axis (left drawing) and Y axis (right drawing). Distances are in mm.

XEN1210-3D board

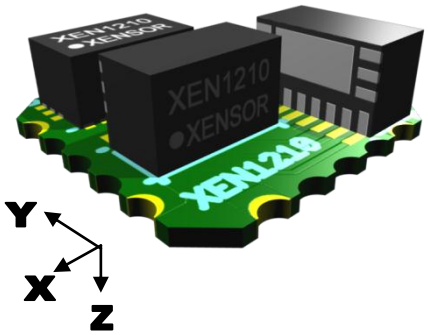


Figure 3: The 3D board consists of three XEN1210 sensors mounted in three orientations to measure the magnetic field in 3D. The devices are daisy chained in the order x,y,z and operate as one. The PCB has the dimensions and connections of a LCC20 package. The size is 8.9x8.9x3.2 mm.

Table 2: XEN-1210-3D board pin definition.

Pin	Name	Type	Functionality
18	CLK	Dig. In	CLocK is the main clock frequency and determines the speed of the module. Typical clock frequency is 1-5MHz.
19	CS	Dig. In	Chip Select selects the device when this input is low. A high level deselects the device and forces SDO into tri-state mode.
20	SCK	Dig. In	Serial shift ClocK determines the speed of the SDI/SDO shift register.
1	SDO	Tri-state Out	Serial Data Output pin. Data is shifted out on the positive edge of SCK.
2	DV	Dig. Out	The Data Valid pin is pulled down when the internal shift register is refreshed with new data. It can be used as an interrupt signal for the µP.
3	GND	Power	Analog and Digital Ground
4	VDD	Power	Analog and Digital Power Supply (2.5V - 3.3V)
8	SDI	Dig. In	Serial Data Input pin. Data shifted in is committed on the falling edge of SCK.

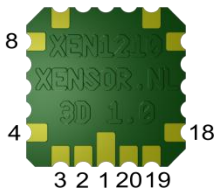


Figure 4: XEN1210-3D board seen from the bottom, with pin numbering according to LCC-20 footage.

Ordering information

Table 3: Ordering number.

Ordering number	Product
XEN1210-3D board	3D LCC20 PCB board
XEN1210-Xaxis	XEN1210 experimentation board
XEN1210--Zaxis	XEN1210 experimentation board

General Information

Product Status

The XEN1210 prototype boards are only available in small numbers.
Customers are encouraged to check for further product developments. Please contact Sensixs Design for further details.

Right to make changes

Sensixs Design reserves the right to make changes to improve reliability, function or design of the devices. Sensixs Design assumes no responsibility or liability for the use of this product.

Application Information

Applications that are described herein are for illustrative purposes only. Sensixs Design makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Life critical applications

These products are not qualified for use in life support applications, aeronautical applications or devices or systems where malfunction of these products can reasonably be expected to result in personal injury

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